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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,493	02/23/2004	Christophe Chevallier	400.069US04	2156

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,493	CHEVALLIER, CHRISTOPHE	
	Examiner	Art Unit	
	Viet Q Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Application filed on 2/23/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-13,16 and 17* is/are rejected.

7)☒ Claim(s) *2,9,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-17** are present for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1, 3-8, 10-13, and 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tran et al (6,282,145).**

Tran et al (see Fig.4A) teaches a flash memory system which includes an array of flash cells, each cell represented by transistors (220 to 227). Col. 18 (see lines 9-42) further describes in detail the internal structure for such array, which includes the use of parallel local bit lines (**SBL0 and SBL1, 240A, 240B, 241A, 241B**) for connecting all the adjacent cells in a local segment (220 to 227). For example, in this embodiment, one can see that the **first local** bit line is line (**240A**), **second local** bit line is bit line (**241A**), **third local** bitline is line (**240B**), **fourth local** bitline is line (**241B**), **first global** bit line is line (**240**), **second global** bit line is line (**241**). It is further seen as the **first select transistor is transistor (220)** for coupling first local line (240A) to first global line (240), **second transistor is transistor (222)** for coupling second local line (241A) to the second global line (241), **third transistor is transistor (221)** for coupling

third local line (240B) to the first global line (240), **and fourth transistor is transistor (223)** for connecting fourth local line (241B) to second global line (241). It is further noted that all four local bit liens are positioned generally in parallel with each other, and a first select line (261) is used to activate the first and second select transistors (220, 222) as claimed. Additionally, a second select line (26) is also used to activate the third and fourth transistors (221, 223) as recited.

Regarding the claimed bit lien arrangement, Fig. 5A also shows that the local bit lines (240 and 241) are formed on a first metal layer (M1), and the global or top bit lines (240-241) are formed on the a higher, second metal layer (M2).

Regarding the claimed "multiplex" circuit, Fig. 26 further shows the use of a multiplexer circuit (26) positioned adjacent to the flash memory cell array (see through data lines DIN).

Fig. 1A also shows that each such flash cell is composed of a floating gate (100F), and control gate (100C), which is capable of holding a charge determining a storing state (see Col. 4-5).

Fig. 4A shows that each global line accommodates 2 local lines or the number of local lines is twice the number of global lines as claimed.

3. Other claims (**2, 9, 14, 15**) contain allowable subject matter over prior arts in view of the claimed "alternate" connection, second multiplex use, and opposite end arrangement of select transistors.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2818

V. Nguyen
11/18/2004